REMARKS

The present response is intended to be fully responsive to all points raised by the Examiner in the Office Action and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

The application as examined includes claims 27 – 38, 40 – 51, and 71 – 78. In the present response, claims 27, 42, and 49 are amended. Claims 28 – 38, 40 – 41, 43 – 48, 50 – 51, and 71 – 78 are unchanged. No additional claims are canceled, and no new claims are added.

Support for amendments to the claims is set forth hereinbelow, with reference to the application as published in U.S. Patent Application Publication No. 2003/0130831:

> The feature recited in amended independent claims 27, 42, and 49 as a "multi-processor design" and a "multi-processor architecture" is disclosed *inter alia* in paragraph **[0015]**:
>
> > **[0015]** "A design verification system, which verifies the operation of ***a multi-processor architecture*** by generating test programs in which the behavior of the processor, when executing the test program, is evaluated against the behavior required by the design specification. The test program generator produces scenarios for ***a multi-processor design*** in which non-unique results may occur..." (emphasis added)

Claims 27 – 38, 40 – 51, and 71 – 78 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Claims 27 – 38, 40 – 51, and claim 72 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Genesys-MP User's Guide ("Genie") in view of "Functional Verification of a Multiple-Issue, Out-of-Order, Superscalar Alpha Processor — The DEC Alpha 21264 Microprocessor" ("Taylor").

Claims 71 and 73 – 78 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Genie in view of Taylor in view of "Development and Validation of a Hierarchical Memory Model Incorporating CPU and Memory-Overlap" ("Luo").

The present invention provides a computer program product for validating a multi-processor design by simulating program execution for a test program having at least two simulated processes which access mutually-dependent non-adjacent resources, and by creating one or more tagged value-lists incorporating a set of non-unique values associated with a combination identifier identifying a particular outcome of the test program. The contents of the resources are then compared with the non-unique values in the tagged value-lists to validate the processor design for the test program.

Genie describes the use and operation of the "Genesys" multi-processor test system.

Taylor describes a simulation-based functional verification of a pipelined superscalar processor featuring out-of-order instruction execution.

Luo describes a "memory-centric" model for use in analyzing and characterizing multi-processor computer systems.

35 U.S.C. §112 Rejection

The Examiner states that the limitation "replacing said set of value-lists by said set of tagged value-lists" is vague and indefinite. The Office Action states (page 2):

> 'It is unclear what the term "replacing" means within the context of the limitation. Is the value-list overwritten by the tagged value-list? Is the tagged value-list now used in place of the previously used value-list? Given its broadest, most reasonable interpretation, the Examiner interprets it as using the tagged value-list instead of the value-list.'

The Applicant notes that the term "replacing" in independent claims 27, 42, and 49, derives from the specification of the present application, paragraph **[0227]**:

> **[0227]** "...The result syntax is now modified as follows. *The set of value-lists is replaced by a set of tagged value-lists* (set-of-tagged-value-lists)." (emphasis added)

The Applicant further notes that a commonly-accepted definition of the word "replace" is "to take the place of especially as a substitute or successor" (Webster).

Therefore, the Applicant is overcoming the 35 U.S.C. §112 rejection by amending independent claims 27, 42, and 49 according to the interpretation as stated in the Office Action, by reciting "such that said set of tagged value-lists is used in place of said set of value-lists".

35 U.S.C. §103(a) Rejections

The Office Action notes that:

> "Genie does not explicitly disclose creating by the computer executing said test program, a set of tagged value lists..." (Office Action, page 4)

The Office Action, however, asserts that Taylor teaches "creating a set of tagged value-lists":

> "section 2 3rd paragraph: the state of the reference model is equivalent to the claimed value-list, since it represents what the output should be, and the state of the RTL model is equivalent to the combination identifier since it represents the actual outcome." (Office Action, page 4)

The Office Action further asserts that Taylor teaches "replacing said set of value-lists by said set of tagged value-lists:

> "section 2 3rd paragraph: verification of the RTL model accomplished by comparing outcome of its state (combination identifier) with that of reference model (value list)." (Office Action, page 4)

The Applicant respectfully disagrees with the above assertions, on the grounds that Taylor is not relevant to the present invention; and that the Office Action misinterprets the teachings of Taylor.

The Applicant first notes that the present invention is direct to the testing of *multi-processor systems*, where race conditions between different concurrently-executing processes can lead to non-unique values of data. If several different processes access shared resources (such as memory or hardware registers), the values of data in those resources can vary, depending on the order in which the processes access the shared resources. This order is not predictable and in general may be different each time the processes are executed. That is, *the data values in the shared resources of a multi-processor system are non-deterministic*.

As put forth in the present application in paragraph **[0009]**:

> **[0009]** "Verification of multiprocessor designs present special complexities, because of *race conditions* that can occur in different registers and other memory stores, ***such that results are unpredictable and non-unique***." (emphasis added)

The present invention is directed to verifying that a multi-processor system is operating correctly, taking into consideration that the multiple processes will naturally create a variety of non-unique data values. Independent claim 27, for example, recites "said tagged value-list comprising: said set of non-unique values".

In contrast, Taylor is directed to the testing of a *single processor system* where such race conditions do not occur. The data values of the resources of Taylor's single processor system are therefore deterministic, and Taylor is not concerned with non-unique values. In particular, ***Taylor fails to disclose a value-list comprising a set of non-unique values***.

Moreover, Taylor is specifically directed to the testing of a single pipelined superscalar processor which features out-of-order execution. This particular architecture is at a lower level from the multi-processor architecture of the present invention, and has design considerations which are entirely different from those of multi-processor architecture. Taylor is concerned with combining and coordinating different simulation models, such as the "Instruction-Set Processor" (ISP) model and the "Register Transfer Level" (RTL) model.

The Applicant respectfully notes that the above-quoted statement from page 4 of the Office Action (that "the state of the reference model is equivalent to the claimed value-list, since it represents what the output should be, and the state of the RTL model is equivalent to the combination identifier since it represents the actual outcome") is incorrect. The state of the (ISP) reference model is *not* equivalent to the value-list, because the ISP reference model does not consider non-unique data values. The state of the RTL (Register Transfer Level) model does *not* represent "the actual outcome", but rather is a different formalism for simulation which Taylor compares against the ISP model to verify the RTL model. The RTL model does not consider non-unique data values, either.

In addition, the Applicant respectfully notes that Taylor's ***comparing*** of values is not the same as the present invention's ***replacing*** of value-lists by tagged value-lists.

To further distinguish the present invention from Taylor, independent claims 27, 42, and 49 are amended to recite "a *multi-processor* architecture test program", as it has been noted that Taylor is restricted to *single-processor* architecture test programs.

The Applicant respectfully submits that the art of record fails to show or suggest at least the following features recited in amended independent claims 27, 42, and 49:

> a multi-processor architecture test program;
>
> creating, by the computer executing said test program, a tagged value-list comprising said set of non-unique values and a combination identifier identifying a particular outcome of said test program;
>
> replacing a set of lists of values by a set of tagged value-lists; and
>
> validating the processor design if a content of said resource is equal to a member of one of said set of tagged value-lists.

The Applicant therefore respectfully submits that amended independent claims 27, 42, and 49 are patentable over the art of record. The remainder of the claims

each depend directly or ultimately from the amended independent claims, and therefore are also allowable over the art of record.

In view of the foregoing remarks, all of the claims are believed to be in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Please charge any fees associated with this response to Deposit Account 09-0468.

Respectfully submitted,

By: /Suzanne Erez/
Suzanne Erez
Reg. No. 46,688
Phone No. 1-888-260-5928

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IBM Corporation
Intellectual Property Law Dept.
P. O. Box 218
Yorktown Heights, New York 10598